P26324

MAT-8219US PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Michio Fukuoka et al. : Art Unit:
Serial No.: 10/032,861 : Examiner:
Filed: December 27, 2001
FOR: CIRCUIT PROTECTOR

VERIFICATION OF A TRANSLATION

Assistant Commissioner for Patents
Washington, D.C. 20231
SIR :

I, the below named translator, hereby declare that:

1. My name and post office address are as stated below.

2. That I am knowledgeable in the English language and in the language of JP2000-397686, and I believe the attached English translation to be a true and complete translation of JP2000-397686.

3. The document for which the attached English translation is being submitted is a patent application on an invention entitled CIRCUIT PROTECTOR.

4. A copy of JP2000-397686 was filed in the U.S. Patent and Trademark Office on December 27, 2001.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Date: 27 February, 2004

Katsuyuki Hirano

Full name of the Translator

K. Hirano

Signature of the Translator

c/o AIN Co., Ltd., Kyo-oto-Bldg., 3rd Floor, 4-6-12,
Hirano-machi, Chuo-ku, Osaka-shi, Osaka, Japan

Post Office Address

[NAME OF THE DOCUMENT] Patent Application
[ARRANGEMENT NUMBER] 2913021268
[DATE OF FILING] December 27, 2000
[ADDRESS] Director-General of the Patent Office
[INTERNATIONAL PATENT CLASSIFICATION] H01H 37/76
[TITLE OF THE INVENTION] Circuit Protector
[NUMBER OF CLAIMS] 1

[INVENTORS]
[NAME] Michio FUKUOKA
[ADDRESS] c/o Matsushita Electric Industrial Co., Ltd.
1006, Oaza-Kadoma, Kadoma-shi, Osaka-fu
[NAME] Kenichi HASEGAWA
[ADDRESS] c/o Matsushita Electric Industrial Co., Ltd.
1006, Oaza-Kadoma, Kadoma-shi, Osaka-fu
[NAME] Eizo HATANAKA
[ADDRESS] c/o Matsushita Electric Industrial Co., Ltd.
1006, Oaza-Kadoma, Kadoma-shi, Osaka-fu
[NAME] Hideyuki TODAKA
[ADDRESS] c/o Matsushita Electric Industrial Co., Ltd.
1006, Oaza-Kadoma, Kadoma-shi, Osaka-fu
[NAME] Yasuki NAGATOMO
[ADDRESS] c/o Matsushita Electric Industrial Co., Ltd.
1006, Oaza-Kadoma, Kadoma-shi, Osaka-fu

[APPLICANT]
[INDENTIFICATION NUMBER] 000005821
[NAME] Matsushita Electric Industrial Co., Ltd.
[ADDRESS] 1006, Oaza-Kadoma, Kadoma-shi, Osaka-fu
[POSTAL CODE] 571-8501

[AGENT]

[IDENTIFICATION NUMBER] 100097445

[NAME] Fumio IWAHASHI, Patent Attorney

[ADDRESS] c/o Matsushita Electric Industrial Co., Ltd.
1006, Oaza-Kadoma, Kadoma-shi, Osaka-fu

[POSTAL CODE] 571-8501

[SELECTED AGENT]

[IDENTIFICATION NUMBER] 100103355

[NAME] Tomoyasu SAKAGUCHI, Patent Attorney

[ADDRESS] c/o Matsushita Electric Industrial Co., Ltd.
1006, Oaza-Kadoma, Kadoma-shi, Osaka-fu

[POSTAL CODE] 571-8501

[SELECTED AGENT]

[IDENTIFICATION NUMBER] 100109667

[NAME] Hiroki NAITO, Patent Attorney

[ADDRESS] c/o Matsushita Electric Industrial Co., Ltd.
1006, Oaza-Kadoma, Kadoma-shi, Osaka-fu

[POSTAL CODE] 571-8501

[REPRESENTATION OF FEE]

[PAYING METHOD] In-advance payment

[NUMBER IN LEDGER OF IN-ADVANCE PAYMENT] 011305

[AMOUNT] 21000

[LIST OF ARTICLES FILED]

[NAME OF ARTICLE] Specification 1

[NAME OF ARTICLE] Drawing 1

[NAME OF ARTICLE] Abstract 1

[NUMBER OF GENERAL POWER OF ATTORNEY] 9809938

[Name of the Document] Specification

[Title of the Invention] Circuit Protector

[What is Claimed is]

[Claim 1] A circuit protector comprising a columnar substrate, a conductive layer disposed on said substrate, a groove which forms a narrow portion formed on the conductive layer of said conductive layer, and a terminal portion disposed at both ends of said substrate, wherein a pore area per unit area of a surface of said substrate or a portion near the surface of said substrate ranges from 1% to 30%.

[Detailed Description of the Invention]

[0001]

[Field of the Invention]

The present invention relates to a circuit protective element used in electronic equipment or mobile electronic equipment mounted with a battery or the like, and particularly, used in a memory storage for a hard disk drive, an optical disk drive or the like, and a personal computer and a mobile personal computer.

[0002]

[Prior Art]

A conventional circuit protective element is disclosed, for example, in Japanese Laid-open Patent H5-120985.

[0003]

In prior art, a pair of conductors are provided on an insulating substrate, a fuse portion is provided over the pair of conductors, a JCR coat portion is provided to cover the fuse portion, and a resin mold portion is

provided to cover the JCR coat portion.

[0004]

[Problems to be Solved by the Invention]

However, in the conventional configuration, the structure is very complicated, and the variation of fusing characteristics is relatively considerable.

[0005]

The present invention is intended to solve the above problems of the prior art, and the object is to provide a circuit protector which may lessen the variation of fusing characteristics.

[0006]

[Means to Solve the Problems]

In the present invention, a conductive layer is disposed on a columnar substrate, and the conductive layer is provided with a groove to dispose a narrow portion thereon, and a pore area per unit area of a surface of the substrate or a portion near the surface of the substrate ranges from 1% to 30%.

[0007]

[Preferred Embodiments of the Invention]

The invention of claim 1 is a circuit protector comprising a columnar substrate, a conductive layer disposed on the substrate, a groove which forms a narrow portion on the conductive layer of the conductive layer, and a terminal portion disposed at both ends of the substrate, wherein a pore area per unit area of a surface of the substrate or a portion near the surface of the substrate ranges from 1% to 30%. Accordingly, the conductive layer

can be properly formed and it is possible to lessen the defects of the narrow portion formed on the conductive layer and to suppress the variation of fusing characteristics.

[0008]

Fig. 1 and Fig. 2 are respectively a perspective view and a side view of a circuit protector in one preferred embodiment of the present invention.

[0009]

In Fig. 1, reference numeral 11 is a substrate formed by press machining, extrusion molding or the like of an insulating material, numeral 12 is a conductive layer disposed on the substrate 11, and the conductive layer 12 is formed on the substrate 11 by printing, coating, plating or evaporation process such as sputtering. Reference numeral 13 is a groove disposed in the substrate 11 and conductive layer 12, and the groove 13 is formed by applying a laser beam or the like to the conductive layer 12 or mechanically formed by means of a grindstone or the like. Reference numeral 14 is a protective material coated on the portion where the groove 13 is formed in the substrate 11 and the conductive layer 12. Numerals 15 and 16 are terminal portions where terminal electrodes are formed respectively, and between the terminal portions 15 and 16 are disposed the groove 13 and the protective material 14. Fig. 2 is a structure without a part of the protective material 14.

[0010]

Also, reference numeral 13a is a narrow portion formed between both ends of the groove 13, and the narrow portion 13a is a part of the conductive layer 12. The fusing current is controlled by setting at least one of the

width and thickness of the narrow portion 13a. That is, as the operation, for example, when fusing at the current level of 5A is desired, the material and thickness of conductive layer 12, the width of narrow portion 13a, and the material of substrate 11 are previously calculated through experiments or the like so that the narrow portion 13a fuses at 5A, and thus, the circuit protector is manufactured according to the structure. And, when a specified level of current (for example, 5A) flows, the narrow portion 13a fuses, thereby preventing the circuit board and electronic equipment from being damaged by overcurrent.

[0011]

Reference numerals 13b, 13c are grooves respectively formed between the narrow portion 13a and terminal portions 15, 16, and the grooves 13b, 13c are ㄷ-shaped. Since the grooves 13b, 13c are provided, in case a current higher than the specified level flows in the narrow portion 13a causing it to be heated, the flow of heat toward the terminal portion is controlled and the fusing time can be shortened, thereby suppressing the variation of characteristics. That is, since the grooves 13b, 13c are provided, the conductive layer 12 of relatively good heat conductivity can be cut off and the spread of head can be controlled, and thereby, it is possible to shorten the fusing time or the like, It is not always required to provide the grooves 13b, 13c depending upon the specification and the environment of the product used.

[0012]

Also, the circuit protector of the present embodiment is preferable to be such that the length L1, width L2, and height L3 of the circuit protector are

as follows.

[0013]

L1 = 0.5 to 2.2 mm (preferably, 0.8 to 1.8 mm)

L2 = 0.2 to 1.3 mm (preferably, 0.4 to 0.9 mm)

L3 = 0.2 to 1.3 mm (preferably, 0.4 to 0.9 mm)

When L1 is less than 0.5 mm, it is very difficult to process and unable to improve the productivity. Also, in case L1 exceeds 2.2 mm, the protector element itself is increased in size and it is unable to reduce the size of the circuit board or the like such as a substrate (hereinafter called circuit board) on which electronic circuits or the like are formed, and consequently, electronic equipment or the like mounted with the circuit board or the like cannot be reduced in size. Also, in case L2, L3 are less than 0.2 mm, the protector element itself too much weakens in mechanical strength, and when mounted on a circuit board of an apparatus or the like, breakage of the protector may take place. Also, in case L2, L3 exceed 1.3 mm, the element is too much increased in size, and it is unable to reduce the size of the circuit board or the like and, as a result, the apparatus cannot be miniaturized. L4 (depth of stepped portion) is preferable to be about 20 μm to 100 μm, and if it is less than 20 μm, when the narrow portion 13a is provided with a fusion accelerator and further protective material 14 thereon, then it is necessary to reduce the thickness of the protective material 14, and consequently, the fusion accelerator is affected by shocks in the mounting process or the like and it is sometimes unable to obtain sufficient fusing characteristics. Also, in case L4 exceeds 100 μm, the substrate weakens in mechanical strength, and it may cause breakage of

the element or like trouble to take place.

[0014]

Each component of the circuit protector configured as described above will be described in detail in the following.

[0015]

Fig. 3 is a sectional view of a substrate formed with a conductive layer used for a circuit protector in one preferred embodiment of the present invention. Fig. 4 (a), (b) are respectively a side view and a bottom view of the substrate.

[0016]

First, the shape of the substrate 11 is described.

[0017]

As shown in Fig. 3 and Fig. 4, the substrate 11 comprises central portion 11a whose cross-section is square-shaped so as to be easily mounted on a circuit board or the like, and end portions 11b, 11c whose cross-section is squared shaped, which are integrally disposed at either ends of the central portion 11a. The end portions 11b, 11c, and the central portion 11a are square-shaped in cross-section, but they are preferable to be polygons such as pentagons and hexagons. The central portion 11a is configured at a level lower than the end portions 11b, 11c. In the present preferred embodiment, since the cross-section of the end portions 11b, 11c is nearly square, the circuit protector can be more easily mounted on a circuit board or the like. Also, in the present preferred embodiment, since the groove 13 is formed sideways in the central portion 11a, mounting on the circuit board or the like can be executed in any directions and it is easier to handle. Also,

the central portion 11a is formed with an element portion (groove 13 or protective material 14), and the terminal portions 15, 16 are formed at the end portions 11b, 11c.

[0018]

In the present preferred embodiment, the central portion 11a and the end portions 11b, 11c are nearly square in shape, but they are preferable to be polygons such as pentagons and the like or circular shapes. Further, in the present preferred embodiment, the cross-sections of the central portion 11a and the end portions 11b, 11c are square and identical with each other, but they are preferable to be different in shape from each other. That is, it is preferable that the cross-section of the end portions 11b, 11c is square and the cross-section of the central portion 11a is polygonal or circular. The cross-section of the central portion 11a being circular, it is possible to reliably form the groove 13.

[0019]

Further, in the preferred embodiment, since the central portion 11a is lower in level than the end portions 11b, 11c, when the protective material 14 is coated, the protective material 14 and the circuit board or the like are prevented from coming in contact with the each other, but it is preferable not to make lower the level of the central portion 11a, particularly depending upon the thickness of the protective material 14 or the conditions of the circuit board or the like (a groove is formed in the portion where the circuit board or the like is mounted or the electrode on the circuit board or the like is rising). When the central portion 11a is not lower in level than the end portions 11b, 11c, the substrate 11 is structurally simplified, the

productivity is improved, and further, the mechanical strength of the central portion 11a is improved. Thus, even without lowering the level, it is preferable to be rectangular prism in shape with its cross-section being square in shape, and further, it is preferable to be prism in shape with its cross-section being polygonal.

[0020]

Also, as shown in Fig. 4 (a), the heights Z1 and Z2 of the end portions of the substrate 11 are preferable to satisfy the following conditions.

[0021]

$| Z1 - Z2 | \leq 80$ μm (preferably, 50 μm)

In case the difference between heights Z1 an Z2 exceeds 80 μm (preferably, 50 μm or less), when the element is mounted on the substrate and soldered to a circuit board or the like, the element is pulled to one end portion due to the surface tension of the solder or the like, causing the element to be raised, that is, a Manhattan phenomenon to take place at a very high percent probability. A side view showing the Manhattan phenomenon is shown in Fig. 5. As shown in Fig. 5, the circuit protector is disposed on substrate 200, and solders 201, 202 are respectively provided between the terminal portions 15, 16 and the substrate 200, but when the solders 201, 202 are melted by reflow or the like, due to the difference in the amount of application between the solders 201, 202 or the difference in melting point because of different materials, the surface tensions of the solders 201, 202 melted are different at the terminal portion 15 and the terminal portion 16, and as a result, as shown in Fig. 5, the circuit protector turns about one of the terminal portions (terminal portion 15 in Fig. 5) to be

raised. In case the difference between heights Z1 and Z2 exceeds 80 μm (preferably, 50 μm or less), the element is disposed on the substrate 200 as it is slanted, causing the element to be promoted in being raised. Also, a Manhattan phenomenon takes place in compact, light-weight chip-type electronic parts (including chip-type circuit protectors) in particular, and moreover, as one of the causes of this Manhattan phenomenon, it is noticeable that the element is disposed in a state of being slanted on the substrate 200 due to the difference in height between the terminal portions 15, 16. Consequently, forming the substrate 11 in such manner as to make the difference between heights Z1 and Z2 less than 80 μm (preferably, 50 μm or less), it is possible to greatly suppress the generation of the Manhattan phenomenon. The generation of Manhattan phenomenon can be almost prevented by making the difference between heights Z1 and Z2 less than 50 μm.

[0022]

Next, chamfering of the substrate 11 will be described.

[0023]

Fig. 6 is a perspective view of a substrate used for a circuit protector in one preferred embodiment of the present invention. As shown in Fig. 6, edges 11e, 11d of end portions 11b, 11c of substrate 11 are chamfered, and as to the radius of curvature R1 of the chamfered edges 11e, 11d and the radius of curvature R2 of the edge 11f of central portion 11a, it is preferable to be formed as follows.

[0024]

$0.03 < R1 < 0.15$ (mm)

$0.01 < R2$ (mm)

In case R1 is 0.03 or less, the edges 11e, 11d become pointed, and slight shocks may cause the edges 11e, 11d to crack, and it may result in deterioration of the characteristics or the like. Also, in case R1 exceeds 0.15 mm, the edges 11e, 11d become too much round, and it may cause the Manhattan phenomenon to take place, resulting in occurrence of trouble. Further, in case R2 is 0.01 mm or less, the edge 11f is liable to have burrs, and they are formed on the central portion 11a, and in addition, the conductive layer 12 that is closely related with the characteristics of the element becomes different in thickness from the edge 11f at the flat surfaces, resulting in increased variation of the element characteristics.

[0025]

Next, the component materials of the substrate 11 will be described. The component materials of the substrate 11 are desirable to satisfy the following characteristics.

[0026]

Next, the component materials of the substrate 11 will be described. The component materials of the substrate 11 are desirable to satisfy the following characteristics.

[0027]

Volume resistivity: 10^{13} Ωm or over (preferably, 10^{14} Ωm or over)

Thermal expansion coefficient: 5×10^{-4}/°C or less (preferably, 2×10^{-5}/°C or less) [thermal expansion coefficient at 20°C to 500°C]

Bending strength: 1300 kg/cm^2 or over (preferably, 2000 kg/cm^2 or less)

Density: 2 to 5 g/cm^3 (preferably, 3 to 4 g/cm^3)

In case the volume resistivity of the component material of substrate 11 is 10^{13} Ωm or less, when a considerable current flows therein, the current begins to flow in the substrate 11 as well, and then the function of the circuit protector will become insufficient.

[0028]

Also, in case the thermal expansion coefficient is 5×10^{-4}/°C or over, the substrate 11 may crack due to heat shocks or the like. That is, in case the thermal expansion coefficient is 5×10^{-4}/°C or over, the groove 13 is formed by using a laser beam, grindstone or the like, then the substrate 11 is locally increased in temperature, and the substrate 11 may be sometimes cracked. However, when the thermal expansion coefficient is as specified above, the generation of cracks can be greatly suppressed and it is possible to prevent the deterioration of the conductive layer 12 and the variation of the fusing characteristics.

[0029]

In case the bending strength is 1300 kg/cm^2 or less, element breakage or the like may take place when mounted on a circuit board or the like by means of a mounting device.

[0030]

In case the density is 2g/cm^3 or less, the substrate 11 is increased in water absorption, causing the characteristics of the substrate 11 to be greatly deteriorated and the characteristics as an element to worsen. Also, in case the density is 5g/cm^3 or over, the substrate increases in weight and there arises a problem of mountability. Particularly, when the density is set within the above-mentioned range, the water absorption is less and

there is almost no intrusion of water into the substrate 11 which is therefore decreased in weight, and there arises no problem when mounted on the substrate by means of a chip mounter.

[0031]

In this way, specifying the volume resistivity, thermal expansion coefficient, bending strength, and density of the substrate 11, it is possible to suppress the variation of characteristics and the generation of cracks in the substrate 11 due to heat shocks or the like. Accordingly, since the fraction defective can be reduced, and further, the mechanical strength can be improved, mounting on a circuit board or the like can be executed by using a mounting device and it is possible to obtain excellent effects such as the improvement of productivity.

[0032]

As a material capable of obtaining the above characteristics, a ceramic material using alumina as main component can be mentioned. However, only using a ceramic material based on alumina is not enough to obtain the above characteristics. That is, since the above characteristics vary depending upon the press pressures, burning temperatures, and additives for forming the substrate 11, it is necessary to properly adjust the manufacturing conditions or the like. Specifically, press pressures 2 to 5t, burning temperatures 1500 to 1600°C, and burning time 1 to 3 hours for machining of the substrate 11 can be mentioned as the manufacturing conditions.

[0033]

Next, the surface roughness of the substrate 11 will be described.

Surface roughness in the following description is the average surface roughness at the center line without exception, and the roughness in the description of conductive layer 12 or the like is also the average roughness at the center line.

[0034]

The surface roughness of substrate 11 is about 0.15 to 1.0 μm, and preferably, about 0.2 to 0.8 μm. Fig. 7 is a graph showing the surface roughness and peeling rates of the substrate used for the circuit protector in one preferred embodiment of the present invention. Fig. 7 is the results of the experiment shown in the following. The substrate 11 and the conductive layer 12 are respectively made of alumina and copper, and the samples are manufactured by changing the surface roughness of the substrate 11, and the conductive layer 12 is formed on each of the samples under the same conditions. Each sample is subjected to ultrasonic cleaning, and after that, the surface of the conductive layer 12 is observed to check for peeling of the conductive layer 12. The surface of the substrate 11 is measured by a surface roughness measuring unit (Tokyo Seimitsu Surfcom Co.: 574A) whose end R is 5 μm. As is obvious from the result, when the average surface roughness is 0.15 μm or less, the peeling rate of conductive layer 12 formed on the substrate 11 is about 5%, and it is possible to obtain reliable bonding strength of the substrate 11 and the conductive layer 12. Further, when the surface roughness is 0.2 μm or over, there is almost no peeling of the conductive layer 12, and if possible, the surface roughness of the substrate 11 is preferable to be 0.2 μm or over. Since the peeling of conductive layer 12 is closely related with the deterioration of element

characteristics, the pealing rate is preferable to be 5% or less from the yield point of view or the like.

[0035]

Also, the surface roughness is preferable to be different between the end portion 11b, 11c and the central portion 11a. That is, within the surface roughness ranging from 0.15 to 0.5 μm, the average surface roughness of end portion 11b, 11c is preferable to be less than the average roughness of central portion 11a. Since the end portions 11b, 11c are laminated with the conductive layer 12 as described above in order to form the terminal portions 15, 16, the surface roughness of the conductive layer 12 formed on the end portions 11b, 11c can be lessened by making the end portions 11b, 11c less in surface roughness than the central portion 11a. Accordingly, the tightness with the electrode of a circuit board or the like can be improved and the circuit protector can be reliably bonded to a circuit board or the like. Also, since the conductive layer 12 is laminated on the central portion 11a and formed with the groove 13, when the groove 13 is formed by laser beam or the like, it is necessary to improve the tightness between the conductive layer 12 and the substrate 11 so that the conductive layer 12 will not peel off from the substrate 11. Therefore, it is preferable to make the central portion 11a greater in surface roughness than the end portions 11b, 11c. Particularly, when the groove 13 is formed by laser beam, the temperature rises more abruptly at the portion subjected to laser beam application than at the other portions, and the conductive layer 12 may sometimes peel due to heat shocks or the like. Accordingly, when the groove 13 is formed by laser beam, it is necessary to more enhance the

bonding strength of the conductive layer 12 and the substrate 11 as compared with the other portions.

[0036]

Thus, since the central portion 11a and the end portions 11b, 11c are different in surface roughness, it is possible to assure the tightness with the circuit board or the like and to prevent the conductive layer 12 from peeling off during machining of the groove 13.

[0037]

In the present preferred embodiment, the bonding strength of the conductive layer 12 and the substrate 11 is improved by adjusting the surface roughness of the substrate 11, but it is possible, for example, to improve the tightness between the conductive layer 12 and the substrate 11 without adjusting the surface roughness in such manner that an intermediate layer formed of at least either Cr only or an alloy of Cr and other metal is disposed between the substrate 11 and the conductive layer 12. Naturally, when the surface roughness of the substrate 11 is adjusted and, further, the intermediate layer and conductive layer 12 are laminated on the substrate 11, it is possible to obtain higher tightness between the conductive layer 12 and the substrate 11.

[0038]

Also, as to the filling densities of the portion where the narrow portion 13a is provided and the other portion of the substrate 11, the other portion is preferable to be lower in filling density. That is, making the filling density lower, it is possible to prevent the diffusion of heat, and the heat generated at the narrow portion 13a is hard to be transferred outside, and

the fusing characteristics can be improved. For example, when the narrow portion 13a is provided at the central portion of the substrate 11, the diffusion of heat can be prevented by making the both ends of the substrate 11 lower in filling density than the central portion.

[0039]

Next, the conductive layer 12 will be described.

[0040]

The conductive layer 12 will be specifically described in the following.

[0041]

As the component materials of conductive layer 12, conductive materials such as copper, silver, gold, nickel, copper alloy, silver alloy, gold alloy, nickel alloy, and aluminum alloy can be mentioned. It is preferable to add a predetermined element to the materials such as copper, silver, gold and nickel in order to improve the weather resistance and the like. Also, it is preferable to use an alloy of conductive material and non-metallic material. Copper and its alloy are often employed as the component materials in view of the cost, wear resistance and easy manufacture. When copper is used as the material of conductive layer 12, a first layer is formed on the substrate 11 by non-electrolytic plating and a predetermined copper layer is formed on the first layer by electrolytic plating, thereby forming the conductive layer 12. Further, when an alloy is used to form the conductive layer 12, it is preferable to adopt a sputtering process or evaporation process. Also, when copper and its alloy (for example, copper-tin alloy) are used as the component material, the forming thickness of the conductive layer 12 is preferable to be 4 μm to 15 μm.

[0042]

The conductive layer 12 can be formed in a single layer, and it is also preferable to be formed in multiple layers. That is, it is preferable to form conductive layers of different component materials. For example, a copper layer is first formed on the substrate 11, and a metallic layer (such as nickel) of good weather resistance is laminated thereon, and thereby, it is possible to prevent the corrosion of copper which is a little poor in weather resistance. Specifically, at least either copper or nickel is formed on the substrate 11, followed by forming silver or the like thereon, and preferably, tin is laminated on the silver or the like.

[0043]

As the forming process of conductive layer 12, a plating process (such as electrolytic plating process and non-electrolytic plating process), sputtering process, and evaporation process can be mentioned. Of these forming processes, a plating process is widely employed because of being excellent in mass-productivity and less in variation of layer thickness.

[0044]

The surface roughness of conductive layer 12 is preferable to be 1 μm or less. Particularly, it is preferable to be 0.2 μm or less. In case the surface roughness of conductive layer 12 exceeds 1 μm, it causes the variation in layer thickness of the conductive layer 12 and the variation of fusing characteristics.

[0045]

The conductive layer 12 in the present preferred embodiment includes a resistance layer such as ruthenium.

[0046]

Protective material 14 will be described in the following.

[0047]

As the protective material 14, an organic material having excellent weather resistance, for example, an insulative material such as epoxy resin is employed. Also, as the protective material 14, it is preferable to be penetrable so that the conditions of groove 13 can be observed. Further, the protective material 14 is preferable to have a specific color as well as penetrability. Coloring the protective material 14 with red, blue or green that is different from the color of the conductive layer 12 or terminal portions 15, 16, it is possible to easily check the distinct parts of the element and to inspect each part of the element. Also, changing the color of the protective material 14 in accordance with the size of the element, characteristics, model number and the like, it is possible to lessen such mistakes that elements different in characteristics or model number are installed in wrong places.

[0048]

Also, it is preferable to apply the protective material 14 so that the length Z1 ranging from the edge of groove 13 to the surface of protective material 14 is 5 μm or over as shown in Fig. 8. In case Z1 is less than 5 μm, characteristic deterioration and discharge are liable to take place, causing the characteristics of the element to be greatly deteriorated. Also, discharge or the like in particular is liable to take place at the edge of groove 13, it is especially preferable to form the protective material 14 of 5 μm or over in thickness on the edge portion. Also, an electrode layer or the

like is sometimes formed by re-plating after forming the protective material 14, but if the protective material 14 of 5 μm or over is not formed on the edge portion, then the electrode layer or the like will be formed on the protective material 14 subjected to trouble when the electrode layer or the like sticks thereto, resulting in deterioration of the characteristics.

[0049]

In the present preferred embodiment, since incombustible member 14a is often subjected to a problem of moisture resistance or strength, there is provided the protective material 14 (such as epoxy resin) having higher moisture resistance and strength in order to solve the problem, but it is not always required to provide the protective material 14 depending upon the conditions such as the using environment, specification and incombustible member 14a.

[0050]

The terminal portions 15, 16 will be described in the following.

[0051]

The terminal portion 15, 16 may display its function with use of only conductive layer 12, but it is preferable to be formed in multiple layers in order to cope with various environmental conditions.

[0052]

Fig. 9 is a sectional view of the terminal portion of the circuit protector in one preferred embodiment of the present invention. In Fig. 9, conductive layer 12 is formed on the end portion 11b of substrate 11, and moreover, protective layer 300 made from material such as nickel and titanium having weather resistance is formed on the conductive layer 12, and also, bonding

layer 301 made from solder, lead-free solder or the like is formed on the protective layer 300. The protective layer 300 is able to improve the bonding strength of the bonding layer and conductive layer 12 and to improve the weather resistance of the conductive layer 12. In the present preferred embodiment, as the component material of the protective layer 300, either nickel or nickel alloy is employed, and as the component material of bonding layer 301, solder or lead-free solder is employed. The thickness of protective layer 300 (nickel) is preferable to be 2 to 7 μm, and if it is less than 2 μm, the weather resistance will worsen, and if it exceeds 7 μm, the protective layer 300 (nickel) itself will become higher in electric resistance, resulting in considerable deterioration of the element characteristics. Also, the thickness of bonding layer 301 (solder) is preferable to be about 5 μm to 10 μm, and if it is less than 5 μm, a solder eating up phenomenon will take place, affecting the bonding of the element and circuit board or the like, and if it exceeds 10 μm, a Manhattan phenomenon is liable to take place, greatly worsening the mountability.

[0053]

The circuit protector configured as described above is free from characteristic deterioration and may assure excellent mountability and productivity.

[0054]

Next, the grooves 13b, 13c will be described.

[0055]

The groove 13b is disposed between the narrow portion 13a and the terminal portion 16. Further, the groove 13c is disposed between the

narrow portion 13a and the terminal portion 15.

[0056]

The grooves 13b, 13c are not formed on the entire periphery, but they are formed over the surface 100 and surfaces 101 and 103 adjacent to the surface 100 shown in Fig. 1. The surface 102 at the opposite side of the surface 100 is not provided with grooves 13b, 13c. That is, the conductive layer 12 formed on the surface 102 is electrically connected with the narrow portion 13a and terminal portions 15, 16.

[0057]

In this way, providing the grooves 13b, 13c, without arranging the conductive layer 12 which is relatively high in heat conduction, heat generated at the narrow portion 13a can be prevented from being diffused to the terminal portions 15, 16. As a result, when the circuit protector is mounted on a circuit board, it is possible to suppress the diffusion of heat from the terminal portions 15, 16 to the circuit board, thereby shortening the fusing time.

[0058]

Also, the width of conductive layer 12 between the ends of groove 13b and the width of conductive layer between the ends of groove 13c (in Fig. 1, grooves 13b 13c are not formed in surface 102, and there exists conductive layer 12 for the width of surface 102) are preferable to be greater than the narrow portion 13a, and in this configuration, it is possible to prevent the electric resistance from increasing. In accordance with a wider concept, the conductive layer 12 regulated by the end of groove 13b connecting the terminal portions 15, 16 to the narrow portion 13a and the conductive layer

12 regulated by the end of groove 13c are preferable to be smaller in electric resistance than the narrow portion 13a. In the present preferred embodiment, since the materials for connections that electrically connect the conductive layer 12 to the terminal portions 15, 16 and the narrow portion 13a are identical with each other, it is important to increase the current flow area, and with the layer thickness of the conductive layer 12 kept constant, the purpose can be easily achieved by regulating the width of conductive layer 12 with the grooves 13b, 13c.

[0059]

Also, in this preferred embodiment, the grooves 13b, 13c are provided over the surfaces 100, 101, 103, but this configuration is not always required. It is also preferable to provide the grooves 13b, 13c only on one surface (for example, surface 100 only) or to provide them on two surfaces (for example, surface 101 and surface 101). That is, the conductive layer 12 positioned between the terminal portions 15, 16 and the narrow portion 13a is provided with non-arrangement portion of conductive layer 12, and thereby, it is configured in that heat generated at the narrow portion 13a is not diffused toward the terminal portions 15, 16.

[0060]

Particularly, as shown in Fig. 1, it is preferable to form the grooves over the surface 100 provided with narrow portion 13a and the surfaces 102, 103 adjacent to the surface 100.

[0061]

Also, it is preferable to form the grooves 13b, 13c at least on the surface 100 provided with the narrow portion 13a. That is, since the

shortest distance from the narrow portion 13a to the terminal portion 15, 16 exists on the surface 100, providing the surface 100 with the grooves 13b, 13c, it is possible to suppress the diffusion of heat generated at the narrow portion 13a and to shorten the fusing time.

[0062]

In the present preferred embodiment, as shown in Fig. 3, the grooves 13b, 13c are formed as much as reaching the substrate 11, but as shown in Fig. 10, it is also preferable to configure in that only the conductive layer 12 is selectively removed by etching and the grooves 13b, 13c are not formed in the substrate 11. Or, as shown in Fig. 11, it is preferable to provide the grooves 13b, 13c so that the conductive layer 12 is not completely removed and the conductive layer 12 is less in thickness than the other portions (preferably, the thickness of the conductive layer of the portion provided with narrow portion 13a). With the grooves 13b, 13c formed, the conductive layer 12 can be partially reduced in thickness, and thereby, the heat transfer area can be decreased. Accordingly, it is possible to suppress the diffusion of heat generated at the narrow portion 13a, and in such a configuration, the grooves 13b, 13c can be formed over the entire periphery (in Fig. 1, all of the surfaces 100, 101, 102, 103), and the diffusion of heat can be further suppressed. Also, the connections of the narrow portion 13a and the terminal portions 15, 16 correspond to the conductive layer 12 remaining on the bottoms of grooves 13b, 13c.

[0063]

Further, in another preferred embodiment, as shown in Fig. 12, with grooves 13b, 13c formed on the entire periphery and the conductive layer 12

divided into the narrow portion 13a side and the terminal portion 15, 16 side, the diffusion of heat at the narrow portion 13a can be most suppressed, but in this case, the electrical connection between the terminal portion 15, 16 and the narrow portion 13a can be achieved by providing the conductive member 110, 111 across each conductive member as shown in Fig. 12. As the conductive member 110, 111, conductive paste, solder, or bar-like, linear, sheet-form, plate-form conductors bonded by conductive material are employed. In this case, if possible, the conductive members 110, 111 are preferable to be disposed at positions apart from the narrow portion 13a. In the preferred embodiment shown in Fig. 12, it is disposed on the surface 102 different from the surface 100 where the narrow portion 13a is disposed. In such a configuration, heat transferred via the conductive members 110, 111 can be further suppressed. Particularly, it is preferable to be disposed on the surface 102 at the opposite side of the surface 100 where the narrow portion 13a is disposed. In the preferred embodiment shown in Fig. 12, the grooves 13b, 13c are provided so as to divide the conductive layer 12, but the increase of electric resistance can be prevented by forming the grooves 13b, 13c so as to connect a part of the conductive layer 12 (in this case, the electric resistance at the connection of the conductive layer 12 becomes very high) and by disposing the conductive members 110, 111.

[0064]

Also, with the grooves 13b, 13c provided, in case the specified characteristics cannot be obtained because of intrusion of foreign matter into the groove, it is preferable to fill a material lower in heat conductivity than the conductive layer 12 into the grooves 13b, 13c. Specifically,

organic material such as resist or silicon resin is used as a preferable material.

[0065]

As described above, providing the grooves 13b, 13c, heat generated at the narrow portion 13a can be prevented from flowing toward the terminal portions 15, 16, and thereby, the fusing time can be shortened. As another result, providing the grooves 13b, 13c, it is also possible to lessen the variation of resistance of the element on the mounting surface. That is, it is also possible to obtain such effect that the variation of resistance value of the element can be lessened by regulating the flow of current between the terminal portion 15, 16 and the narrow portion 13a with the conductive layer 12 (connection) and the conductive member 110, 111 regulated by the grooves 13b, 13c.

[0066]

In the present preferred embodiment, there are provided two grooves, grooves 13b, 13c, as regulating portions, but the diffusion of heat can be decreased at least by one of them.

[0067]

Also, in the present preferred embodiment, grooves such as the grooves 13b, 13c are used as regulating portions, but as shown in Fig. 13, it is preferable to be configured in that a non-arrangement portion 120 of conductive layer 12 or the like is disposed. And, instead of the square non-arrangement portion 120, the non-arrangement portion is also preferable to be circular or oval in shape.

[0068]

Further, as to the space between the groove 13 configuring the narrow portion 13a and the grooves 13b, 13c being the regulating portions, as shown in Fig. 1, when the space of narrow portion 13a is W1, and the space between the groove 13 and the grooves 13b, 13c is W2, it is configured so that W2 ÷ W1 = 1.15 or over, and thereby, stable characteristics can be obtained without increasing the electric resistance. W1 usually ranges from 10 μm to 40 μm in the configuration.

[0069]

Further, the groove width 3 of groove 13 (in Fig. 1, width along the lengthwise direction of the element) is preferable to be less than 45 μm. Also, with respect to the characteristics and productivity, W3 is preferable to be larger than 6 μm. That is, at least the width W3 of groove 13 that determines the narrow width 13a being the fusing portion is preferably 6 μm < W3 < 45 μm (more preferably, 11 μm < W3 < 40 μm).

[0070]

That is, in the actual manufacture of mass-produced products, there arose a problem of variation in fusing time of the narrow portion 13a. The narrow portion 13a was observed in detail to find that the narrow portion 13a was thermally damaged. Then, when the groove 13 is formed by laser beam application, it has been found that the width W3 of groove 13 is the cause of thermal damage given to the narrow portion 13a. That is, if it is configured so that the width W3 of the portion where the narrow portion 13a in particular of the groove 13 is formed becomes wider than the specified width, then the output and the focus of the laser beam must be so much enlarged. Consequently, considerable heat is generated when the

groove 13 is formed and the narrow portion 13a is thermally damaged. Fig. 14 is an enlarged view of the groove 13 formed so that the width W3 becomes 48 μm. As is obvious from Fig. 14, the narrow portion 13a between the grooves 13 is thermally damaged and there are some areas of the narrow portion where the color is changed due to heat.

[0071]

In the present preferred embodiment, it has been found that in order to prevent the narrow portion 13a from being thermally damaged, it is necessary to make the groove width W3 less than 45 μm, then the laser beam output can be lessened and the thermal damage to the narrow portion 13a can be suppressed. That is, setting the groove width W3 less than the specified width, the amount of heat generated when the groove 13 is formed can be suppressed, and it is possible to reduce the thermal damage to the narrow portion 13a.

[0072]

Similarly, same holds true when the groove 13 is formed by means of a grindstone, and with the width of the grindstone increased, the generation of frictional heat becomes greater, giving rise to the generation of a similar problem. Accordingly, even when it is formed by using a grindstone, it is important to regulate the width of the groove 13.

[0073]

Fig. 15 shows a state of the groove 13 formed so that the groove width W3 is 16 μm. As is apparent from Fig. 15, there is almost no color change of the narrow portion 13a, and the variation of characteristics in mass-produced products is extremely little. Next, when the groove width

W3 is 48 μm as shown in Fig. 14, and when the groove width W3 is 16 μm as shown in Fig. 15, the variations of the fusing time are as shown in Fig. 16 and Fig. 17. Each of Fig. 16 and Fig. 17 is a graph showing the relationship between the resistance value and fusing time of the element when the rated current of the circuit protector is 0.5A. As is obvious from Fig. 16 and Fig. 17, the variation of resistance value (horizontal axis of the graph) of the element is less when the groove width W3 is 16 μm, and the variation of fusing time (vertical axis of the graph) of the element is less when the groove width W3 is 16 μm, and it is clear that the characteristics of the circuit protector can be improved when 6 μm < W3 < 45 μm with respect to the groove width W3.

[0074]

In order to obtain reliable fusing characteristics, it is preferable to provide a fusion accelerator on the narrow portion 13a. That is, the narrow portion 13a itself has sufficient fusing characteristics, but it is preferable to provide the fusion accelerator on the narrow portion 13a or in the immediate vicinity of the narrow portion 13a in order to reliably lessen the variation of fusing time and the like. Further, providing the fusion accelerator only on the narrow portion 13a or applying the fusion accelerator on the entire periphery of the substrate 11, it is possible to more reliably provide the fusion accelerator on the narrow portion 13a even in case of inaccurate application rather than in the manner of point application. Also, when the fusion accelerator is disposed in the groove 13 configuring the narrow portion 13a, it is configured in that the fusion accelerator comes in contact with the top and side of the narrow portion 13a, and the fusing

characteristics can be reliably obtained. The layers with the fusion accelerator provided are configured in the order of substrate 11, conductive layer 12 (narrow portion 13a), fusion accelerator, and protective material 14.

[0075]

As the fusion accelerator, for example, glass of low melting point containing lead is used.

[0076]

Next, pores formed in the surface of substrate 11 will be described.

[0077]

When the conductive layer 12 is formed on the substrate 11, it is necessary to lessen the defects of the conductive layer 12. That is, if the conductive layer 12 includes many defects, the narrow portion 13a on which the conductive layer 12 is formed will also become defective, causing the variation of fusing characteristics. As a means to form the conductive layer 12 in good quality, it has been found that a good-quality conductive layer can be formed by prescribing the pore area per unit area with respect to the pore formed in the substrate 11.

[0078]

Namely, prescribing that the area occupied by pores per unit area in the surface of substrate 11 or the surface revealed by slicing a portion near the surface of substrate 11 is 1% to 30% (preferably, 8% to 23%), the conductive layer 12 with good quality can be formed. Substrate 11 of which the area occupied by pores is less than 1% is not desirable from the viewpoint of cost and mass-productivity.

[0079]

The surface revealed by slicing a portion near the surface of substrate 11 was observed by a microscope or the like, and the areas of all pores existing per unit area were calculated by image processing to check for the pore area per unit area.

[0080]

Fig. 18 and Fig. 19 are diagrams showing the surface states of substrate 11. In Fig. 18 and Fig. 19, black portions are pores. Shown in Fig. 18 are a large number of pores occupying a large area, whose pore area per unit area is about 43%, and if such substrate 11 is used, the conductive layer 12 formed is poor in quality, causing excessive variation of fusing characteristics. Also, shown in Fig. 19 are a small number of pores occupying a small area, whose pore area per unit area is about 15%, and when such substrate 11 is used, the conductive layer 12 formed is almost free of defects, and it is possible to obtain excellent fusing characteristics. As a result of detailed inspections, it has been found that adequate fusing characteristics can be obtained when the pore area per unit area is 30% or less.

[0081]

Also, as a pore control method, it is easily realized by properly adjusting the forming density of substrate 11, sintering temperature, component (for example, alumina content) and additives. The substrate 11 shown in Fig. 19 comprises, for example, 55% of alumina, and a material containing at least one of SiO_2, Na_2O, MgO, CaO, K_2O, ZrO_2 as additives.

[0082]

Also, in the case of substrate 11 including many pores, an insulative layer of 5.0W/(m·K) in heat conductivity is first formed 0.01 μm to 1.5 μm thick on the substrate 11 by an evaporation or sputtering process, and on the insulative layer is formed the conductive layer 12, thereby reducing pore generation and suppressing heat dissipation, and the fusing characteristics can be improved.

[0083]

As a specific component of the insulative layer, it is preferable to comprises a material formed from at least one of steatite, Kojilite, mullite, forsterite, and SiO_2. Particularly, when an insulative layer formed from SiO_2 is used, the heat conductivity is very low and the pores can be suppressed.

[0084]

The method of manufacturing a circuit protector having a configuration as described above will be described in the following.

[0085]

First, substrate 11 is manufactured by press-forming or extruding, followed by burning, an insulating material such as alumina. Subsequently, conductive layer 12 is formed on the whole of the substrate 11 by a plating process and sputtering process. In this case, if there exist many pores, an insulative layer is formed on the substrate 11 by an evaporation process or the like as described above. Next, spiral grooves 13, 13b, 13c are formed in the substrate 11 with the conductive layer 12 formed thereon. The grooves 13, 13b, 13c are formed by laser-beam machining or cutting. In that case, the grooves 13b, 13c are not always required to be

formed depending upon the specification, but at least the groove 13 must be formed. Since laser-beam machining is excellent in productivity, a laser-beam machining process will be described in the following.

[0086]

Laser such as YAG laser, excimer laser, and carbon dioxide laser can be used, and the laser beam is limited by a lens or the like and applied to central portion 11a of the substrate 11. Further, the depth of groove 13 can be adjusted by regulating the power of the laser, and the width of groove 13 can be adjusted by replacing the lens for limiting the laser beam. Also, since the laser absorption varies with the component of the conductive layer 12, it is desirable to properly select the type of laser (laser beam length) according to the component of the conductive layer 12. In the present preferred embodiment, laser is used for forming grooves, but it is also possible to use a particle beam such as an electron beam. That is, a high-energy beam is employed for forming grooves.

[0087]

In this way, the groove 13 is formed by means of laser in order to make narrow portion 13a. Conductive members 110, 111 are disposed between the conductive layer 12 at that time when the conductive members 110, 111 are to be provided.

[0088]

Next, protective material 14 is applied and dried in accordance with the using environment and specification. When fusion accelerator is provided, the fusion accelerator is provided on the narrow portion 13a before applying the protective material 14.

[0089]

The product is completed at that point, but a nickel layer or solder layer is sometimes laminated on terminal portions 15, 16 in particular for improving the weather resistance and bonding tightness. A nickel layer or solder layer is formed by a plating process or the like on a half-finished produced with protective material 14 formed thereon.

[0090]

[Advantages of the Invention]

In the present invention, a conductive layer is formed on a columnar substrate, and a groove is formed in the conductive layer, thereby making a narrow portion, and a pore area per unit area of a surface of the substrate or a portion near the surface of the substrate ranges from 1% to 305. As a result, it is possible to lessen the defects of the narrow portion formed on the conducive layer and to suppress the variation of fusing characteristics.

[Brief Description of the Drawings]

Fig. 1 is a perspective view showing a circuit protector in one preferred embodiment of the present invention.

Fig. 2 is a side view showing a circuit protector in one preferred embodiment of the present invention.

Fig. 3 is a sectional view of a substrate formed with a conductive layer which is used for a circuit protector in one preferred embodiment of the present invention.

Fig. 4 is a diagram showing a substrate used for a circuit protector in one preferred embodiment of the present invention.

Fig. 5 is a side view showing a Manhattan phenomenon.

Fig. 6 is a perspective view of a substrate used for a circuit protector in one preferred embodiment of the present invention.

Fig. 7 is a graph showing the surface roughness and peeling rate of a substrate used for a circuit protector in one preferred embodiment of the present invention.

Fig. 8 is a side view of a portion with a protective material of a circuit protector in one preferred embodiment of the present invention.

Fig. 9 is a sectional view of a terminal portion of a circuit protector in one preferred embodiment of the present invention.

Fig. 10 is a perspective view showing a circuit protector in another preferred embodiment of the present invention.

Fig. 11 is a side view showing a circuit protector in another preferred embodiment of the present invention.

Fig. 12 is a perspective view showing a circuit protector in another preferred embodiment of the present invention.

Fig. 13 is a perspective view showing a circuit protector in another preferred embodiment of the present invention.

Fig. 14 is an enlarged view of a narrow portion of a circuit protector.

Fig. 15 is an enlarged view of a narrow portion of a circuit protector.

Fig. 16 is a graph showing the relationship between resistance value and fusing time of a circuit protector when the rated current of the element is 0.5A.

Fig. 17 is a graph showing the relationship between resistance value and fusing time of a circuit protector when the rated current of the element is 0.5A.

Fig. 18 is a partly enlarged view of a substrate surface.

Fig. 19 is a partly enlarged view of a substrate surface.

[Description of the Reference Numerals]

11 Substrate

11a Central portion

11b, 11c End portion

11d, 11e, 11f Edge portion

12 Conductive layer

13 Groove

13a Narrow portion

13b, 13c Groove

14 Protective material

15, 16 Terminal portion

50, 51 Stepped portion

100 Fusion accelerator